Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-2. (Cancelled)

3. (Currently Amended) A data recorder for writing data to a recording medium, the data recorder comprising:

a buffer memory for temporarily storing data before the data is written to the recording medium;

an encoder connected to the buffer memory, [~~wherein~~] the encoder being configured to receive[s] data read from the buffer memory and to encode[s] the read data to generate encoded data;

an [~~one or more~~] address memor[~~ies~~]y connected to the buffer memory, [~~wherein~~] the [~~one or more~~] address memor[~~ies~~]y being configured to store a write_data_address of the data written to the recording medium and a read_data_address of the data read from the buffer memory when the writing of data to the recording medium is interrupted, [~~wherein~~] the write_data_address and the read_data_address each indicat[e]ing a location of the data [~~when~~] at which the interruption occurs;

a synchronizing circuit for synchronizing the written data read from the recording medium with the encoded data;

a first retry determination circuit for determining whether an address of the written data, which is read from the recording medium, and the write_data_address, which is stored in the [~~one or more~~] address memor[~~ies~~]y, are the same, and for determining whether an address of the read data, which is provided to the encoder from the buffer memory, and the read data address, which is stored in the [~~one or more~~] address memor[~~ies~~]y, are the same;

a second retry determination circuit for determining whether a first timing signal for

reading the written data from the recording medium and a second timing signal for encoding the read data are the same, the first timing signal being derived from the recording medium; and

a restart circuit for restarting the writing of data to the recording medium based on the determinations of the first and second retry determination circuits.

4. (Currently Amended) The data recorder according to claim 3, wherein the written data read from the recording medium includes a first subcode synchronizing signal and the encoded data includes a second subcode synchronizing signal, and wherein the second retry determination circuit determines whether the first and second timing signals [~~for reading the written data from the recording medium and the timing for encoding the read data~~] are the same based on the first and second subcode synchronizing signals.

5. (Currently Amended) The data recorder according to claim 3, wherein the second retry determination circuit determines whether the first and second timing[~~s~~] signals are the same when the first retry determination circuit determines that the addresses are the same.

6. (Currently Amended) The data recorder according to claim 3, further comprising:

a first location detection circuit connected to the [~~one or more~~] address memor[~~ies~~]y, wherein the first location detection circuit detects whether the address of the written data read from the recording medium and the write-data-address stored in the [~~one of more~~] address memor[~~ies~~]y are the same; and

a second location detection circuit connected to the [~~one or more~~] address memor[~~ies~~]y, wherein the second location detection circuit detects whether the address of the data read from the buffer memory and the read-data-address stored in the one or more address memories are the same.

7. (Currently Amended) A data recorder for writing data to a recording medium, the

data recorder comprising:

a buffer memory for temporarily storing data before the data is written to the recording medium;

an encoder connected to the buffer memory, wherein the encoder receives data read from the buffer memory and encodes the read data to generate encoded data;

an [~~one or more~~] address memor[~~ies~~]y connected to the buffer memory, wherein the [~~one or more~~] address memor[~~ies~~]y stores a write-data-address of the data written to the recording medium and a read-data-address of the data read from the buffer memory when the writing of data to the recording medium is interrupted, wherein the write-data-address and the read-data-address each indicate a location of the data [~~when~~] at which the interruption occurs;

a synchronizing circuit for synchronizing the written data read from the recording medium with the encoded data;

a retry determination circuit for determining whether an address of the written data, which is read from the recording medium, and the write data address, which is stored in the [~~one or more~~] address memor[~~ies~~]y, are the same, and for determining whether an address of the read data, which is provided to the encoder from the buffer memory, and the read data address, which is stored in the [~~one or more~~] address memor[~~ies~~]y, are the same, wherein the synchronizing circuit determines whether a first timing signal for reading the written data from the recording medium and a second timing signal for encoding the read data are the same; and

a restart circuit for restarting the writing of data to the recording medium based on the determinations of the retry determination circuit and the synchronizing circuit.

8. (Currently Amended) The data recorder according to claim 7, wherein the written data read from the recording medium includes a first subcode synchronizing signal and the encoded data includes a second subcode synchronizing signal, and wherein the synchronizing circuit determines whether the first and second timing signals [~~for reading the written data from the recording medium and the timing for encoding the read data~~] are the same based on the first

and second subcode synchronizing signals.

9. (Currently Amended) The data recorder according to claim 7, wherein the synchronizing circuit determines whether the first and second timing[~~s~~] signals are the same when the first retry determination circuit determines that the addresses are the same.

10. (Currently Amended) The data recorder according to claim 7, further comprising:

a first location detection circuit connected to the [~~one or more~~] address memor[~~ies~~]y, wherein the first location detection circuit detects whether the address of the written data read from the recording medium and the write_data_address stored in the [~~one of more~~] address memor[~~ies~~]y are the same; and

a second location detection circuit connected to the [~~one or more~~] address memor[~~ies~~]y, wherein the second location detection circuit detects whether the address of the data read from the buffer memory and the read_data_address stored in the [~~one or more~~] address memor[~~ies~~]y are the same.